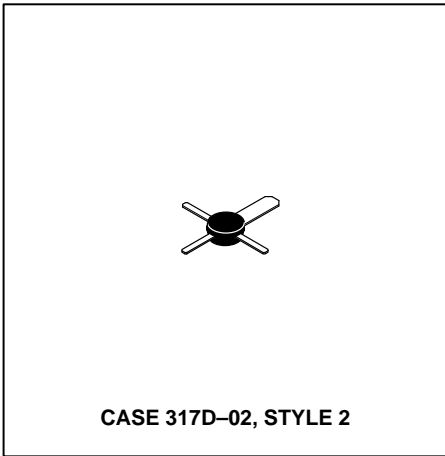
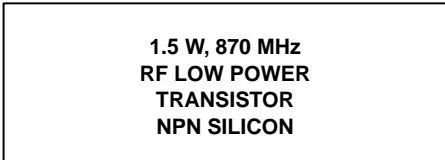


# The RF Line

## NPN Silicon

### RF Low Power Transistor



Designed primarily for wideband large signal predriver stages in the 800 MHz frequency range.

- Specified @ 12.5 V, 870 MHz Characteristics
  - Output Power = 1.5 W
  - Minimum Gain = 8.0 dB
  - Efficiency 60% (Typ)
- Cost Effective PowerMacro Package
- Electroless Tin Plated Leads for Improved Solderability
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	16	Vdc
Collector-Base Voltage	$V_{CBO}$	36	Vdc
Emitter-Base Voltage	$V_{EBO}$	4.0	Vdc
Collector Current — Continuous	$I_C$	400	mAdc
Total Device Dissipation @ $T_C = 75^\circ\text{C}$ (1, 2) Derate above $75^\circ\text{C}$	$P_D$	3.0 40	Watts mW/ $^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55 to +150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	$^\circ\text{C/W}$

#### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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#### OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage ( $I_C = 5.0$ mAdc, $I_B = 0$ )	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage ( $I_C = 5.0$ mAdc, $V_{BE} = 0$ )	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage ( $I_E = 0.1$ mAdc, $I_C = 0$ )	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current ( $V_{CE} = 15$ Vdc, $V_{BE} = 0$ , $T_C = 25^\circ\text{C}$ )	$I_{CES}$	—	—	0.1	mAdc

#### ON CHARACTERISTICS

DC Current Gain ( $I_C = 100$ mAdc, $V_{CE} = 5.0$ Vdc)	$h_{FE}$	50	90	200	—
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#### DYNAMIC CHARACTERISTICS

Output Capacitance ( $V_{CB} = 15$ Vdc, $I_E = 0$ , $f = 1.0$ MHz)	$C_{ob}$	—	3.5	5.0	pF
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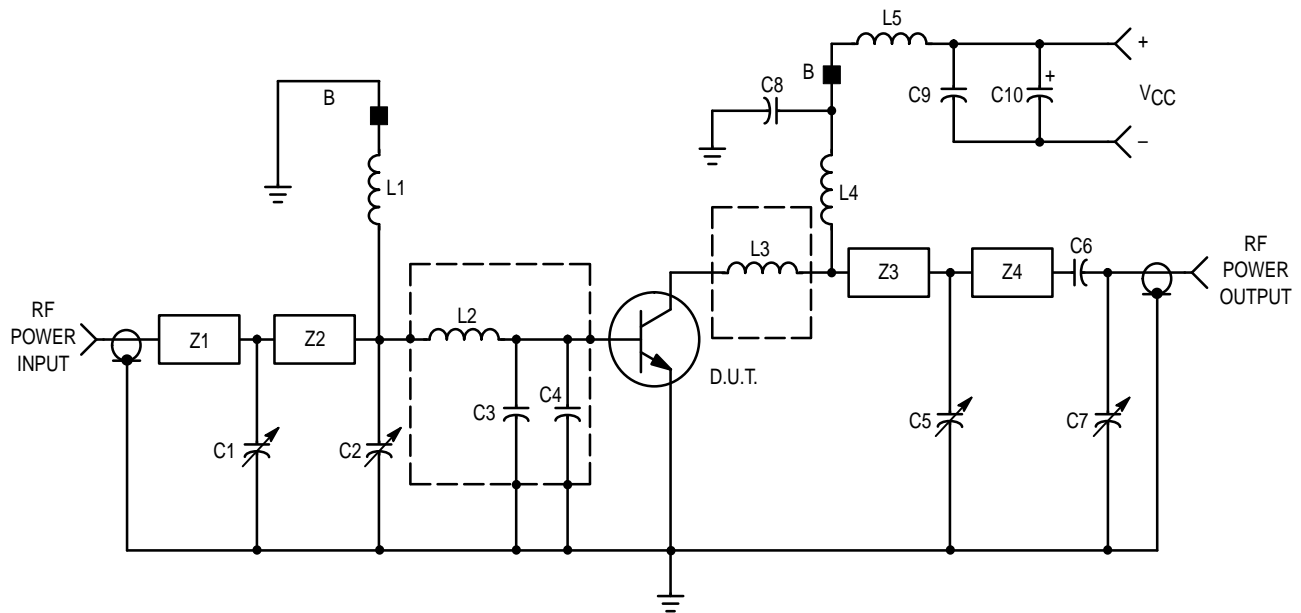
#### NOTES:

- $T_C$ , Case temperature measured on collector lead immediately adjacent to body of package.
- The MRF557 PowerMacro must be properly mounted for reliable operation. AN938, "Mounting Techniques in PowerMacro Transistor," discusses methods of mounting and heatsinking.

(continued)

**ELECTRICAL CHARACTERISTICS — continued** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>FUNCTIONAL TESTS</b>					
Common-Emitter Amplifier Power Gain ( $V_{CC} = 12.5\text{ Vdc}$ , $P_{Out} = 1.5\text{ W}$ , $f = 870\text{ MHz}$ )	Figures 1, 2 $G_{pe}$	8.0	9.0	—	dB
Collector Efficiency ( $V_{CC} = 12.5\text{ Vdc}$ , $P_{Out} = 1.5\text{ W}$ , $f = 870\text{ MHz}$ )	Figures 1, 2 $\eta_c$	55	60	—	%
Load Mismatch Stress ( $V_{CC} = 15.5\text{ Vdc}$ , $P_{in} = 225\text{ mW}$ , $f = 870\text{ MHz}$ , $VSWR \geq 10:1$ all phase angles)	Figures 1, 2 $\psi$	No Degradation in Output Power			



- C1, C2, C5, C7 — 0.8–8.0 pF Johanson Gigatrim\*
- C3, C4 — 15 pF Clamped Mica, Mini-Underwood
- C6 — 27 pF Clamped Mica, Mini-Underwood
- C8 — 91 pF Clamped Mica, Mini-Underwood
- C9 — 68 pF Clamped Mica, Mini-Underwood
- C10 — 1.0  $\mu\text{F}$ , 25 V Tantalum
- B — Bead, Ferroxcube 56-590-65/3B
- PCB — 1/16" Glass Teflon,  $\epsilon_r = 2.56$

- L1, L4 — 5 Turns #21 AWG, 5/32" ID
- L2, L3 — 60 x 125 x 250 Mils Copper Tab on  
27 Mil Thick Alumina Substrate
- L5 — 7 Turns #21 AWG, 5/32" ID
- Z1 — 1.65 x 0.163" Microstrip,  $Z_0 = 50\ \Omega$
- Z2 — 0.85 x 0.163" Microstrip,  $Z_0 = 50\ \Omega$
- Z3 — 0.625 x 0.163" Microstrip,  $Z_0 = 50\ \Omega$
- Z4 — 1.35 x 0.163" Microstrip,  $Z_0 = 50\ \Omega$

\*Fixed tuned for broadband response.

**Figure 1. 800–880 MHz Broadband Circuit**

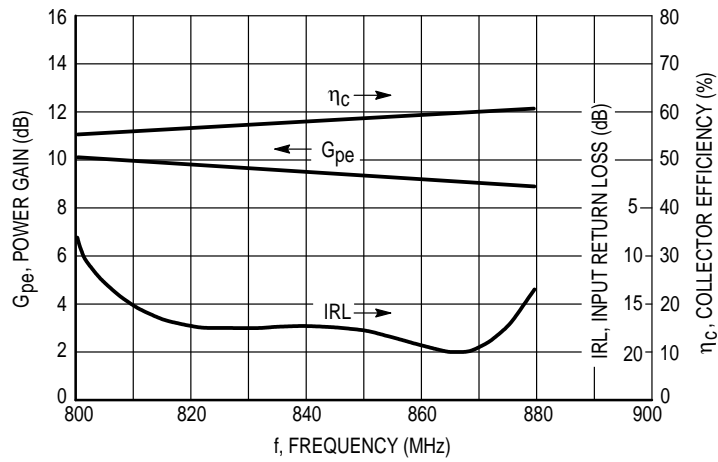


Figure 2. Performance in Broadband Circuit

f Frequency MHz	$Z_{in}$ Ohms		$Z_{OL}^*$ Ohms	
	$V_{CC} = 7.5\text{ V}$	$V_{CC} = 12.5\text{ V}$	$V_{CC} = 7.5\text{ V}$	$V_{CC} = 12.5\text{ V}$
	$P_{in} = 300\text{ mW}$	$P_{in} = 200\text{ mW}$	$P_{out}\ 806\text{ MHz} = 1.7\text{ W}$ $P_{out}\ 870\text{ MHz} = 1.4\text{ W}$ $P_{out}\ 960\text{ MHz} = 1.0\text{ W}$	$P_{out}\ 806\text{ MHz} = 2.1\text{ W}$ $P_{out}\ 870\text{ MHz} = 1.8\text{ W}$ $P_{out}\ 960\text{ MHz} = 1.1\text{ W}$
806	$2.4 + j3.9$	$2.4 + j3.1$	$14.7 - j4.4$	$13.6 - j12.8$
870	$2.5 + j4.6$	$2.7 + j3.7$	$17.2 - j8.6$	$16 - j13.2$
960	$6.1 + j7.4$	$6.8 + j8.3$	$40 - j8.3$	$38 - j10.5$

$Z_{OL}^*$  = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Table 1.  $Z_{in}$  and  $Z_{OL}$  versus Collector Voltage, Input Power and Output Power

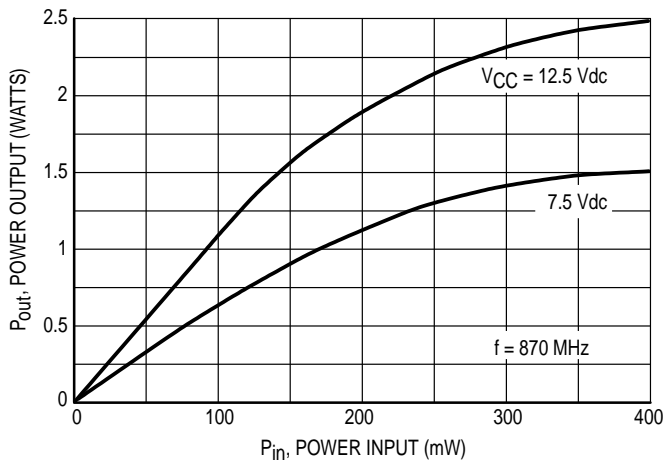


Figure 3. Power Output versus Power Input

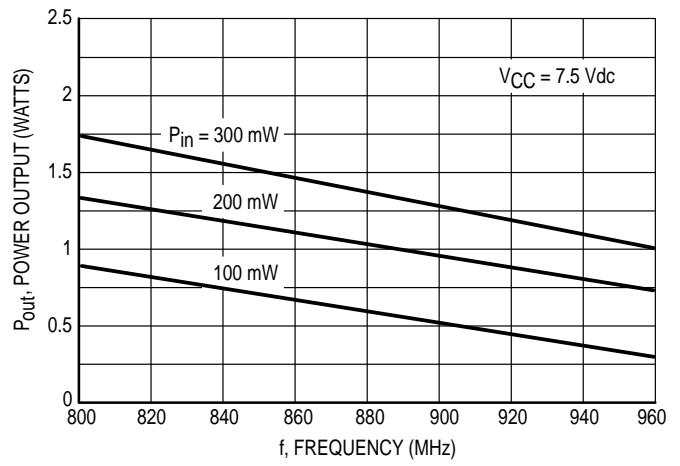


Figure 4. Power Output versus Frequency

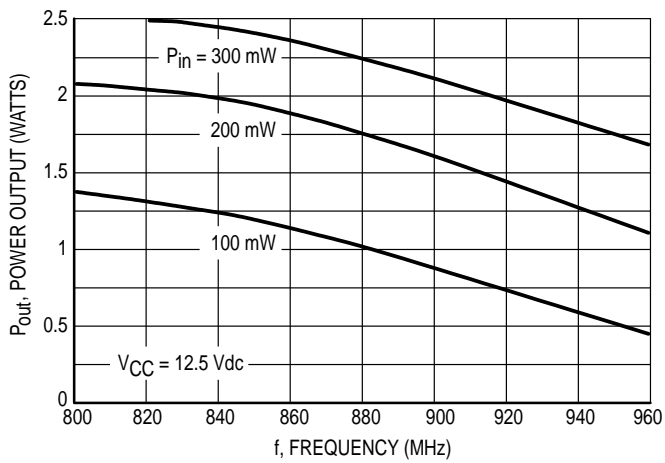


Figure 5. Power Output versus Frequency

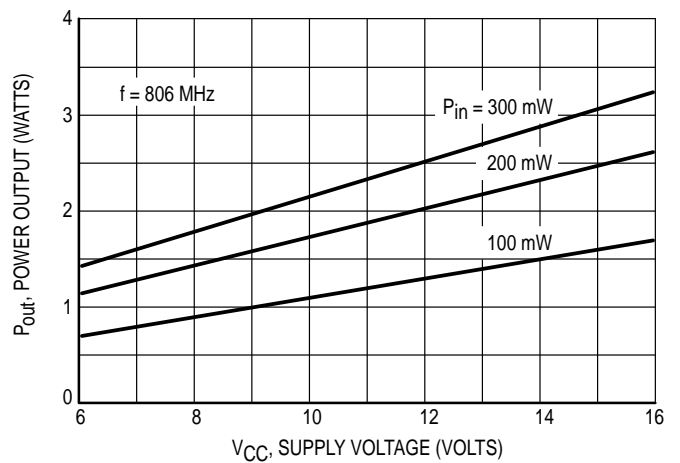


Figure 6. Power Output versus Supply Voltage

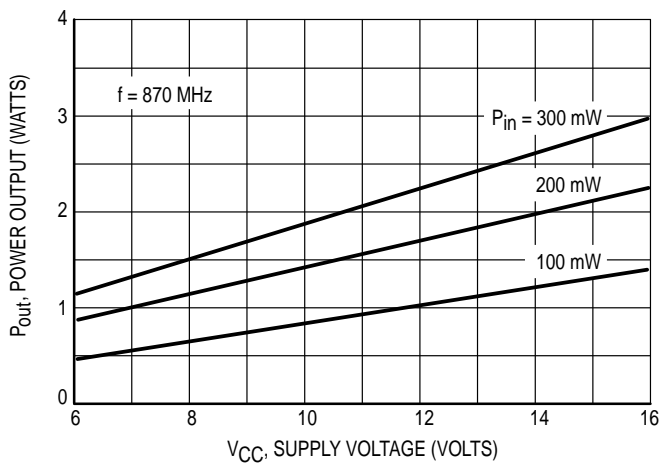


Figure 7. Power Output versus Supply Voltage

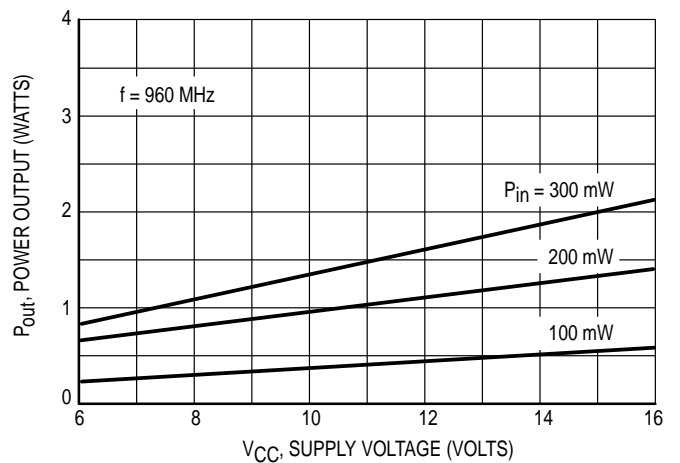
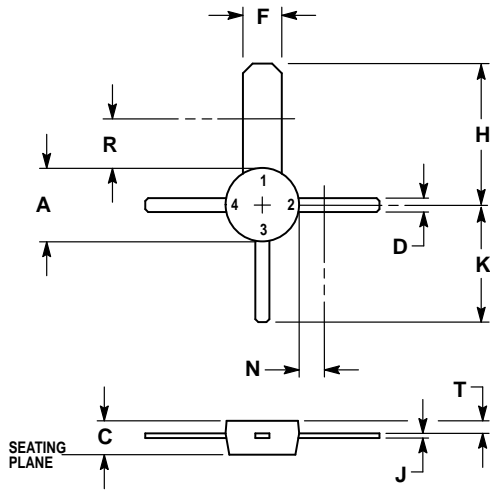


Figure 8. Power Output versus Supply Voltage

# PACKAGE DIMENSIONS




- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.  
 3. LEAD DIMENSIONS UNCONTROLLED WITHIN DIMENSION N AND R.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
C	0.075	0.100	1.91	2.54
D	0.033	0.039	0.84	0.99
F	0.097	0.104	2.46	2.64
H	0.348	0.383	8.84	9.72
J	0.008	0.012	0.24	0.30
K	0.285	0.320	7.24	8.12
N	—	0.065	—	1.65
R	—	0.128	—	3.25
T	0.025	0.040	0.64	1.01

- STYLE 2:  
 PIN 1. COLLECTOR  
 2. EMITTER  
 3. BASE  
 4. EMITTER

**CASE 317D-02  
 ISSUE C**

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